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By: Chen et al.
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Vertical Nano-Transistor, Method of Its Fabrication, and Memory Assembly

Specification

The invention relates to a vertical nano-transistor. A method of its fabrication and a memory assembly.

German laid-open patent specification DE-OS 101 42 913 describes a transistor arrangement resisting mechanical stresses by bending, shearing or stretching in which semiconductor material is vertically introduced into micro-holes of a film composite consisting of plastic films with an intermediate metal layer. The semiconductor material is provided with metallic contacts at the upper and lower surfaces of the film composite. However, the application of a metal layer on a plastic film is no easy matter; moreover, the method of fabricating such a vertical transistor arrangement includes a plurality of individual method steps.

The fabrication of the vertical nano-transistor described by US 2002/0001905 is also complex and complicated, since initially a source region is applied to an expensive semiconductor substrate which is nor flexible onto which an insulating layer is applied. Holes in the nm-range are provided in the insulating layer (Al_2O_3 or Si), and vertically aligned carbon nano-tubes are inserted into these holes. The gate region is arranged above the insulating layer around the carbon nano-tubes and is filled with a non-conductive material up to the upper cover surface of the nano-tubes. Forming the gate region around the nano-tubes and maintaining identical diameters of these nano-tubes during filling has been proven to be very difficult. The result may

be vertical transistor arrangements which because of the different diameters of the relevant nano-tubes are of different characteristics.

It is, therefore, an object of the invention to provide a vertical nano-transistor of good resistance against mechanical stresses and the fabrication of which is of lower complexity than what has hitherto been known in the prior art. A method of fabrication and a memory assembly are to be provided as well.

In accordance with the invention, the object is accomplished by the provision of a vertical nano-transistor having a source region, a drain region, a gate region and a semiconductor channel region between the source region and the drain region, the gate region being formed by a metal film into which the transistor is embedded such that the gate region and the semiconductor channel region form a coaxial structure, the source region, the semiconductor channel region and the drain region being arranged in a vertical direction and the gate region being electrically insulated from the source region, the drain region and the semiconductor channel region.

In the system in accordance with the invention, the gate region is formed by an extremely thin metal film. The extremely difficult application of a metal layer onto a plastic film is avoided; also, unlike in the mentioned arrangement, the individual films need not be assembled into a composite film. The density of the holes formed in the metal film for providing the coaxial structures is very high.

Embodiments of the invention provide for cylindrically structuring the semiconductor channel region. The diameter of the semiconductor channel region amounts to from several ten to several hundred nanometers. The material of the semiconductor channel region is CuSCN or TiO_2 or PbS or ZnO or another compound semiconductor.

The thickness of the metal film forming the vertical gate region amounts to less than 100 µm, preferably 5 to 20 µm. Compared to plastic film, the height of the metal film is more uniform which, given the small thickness, ensures that the inserted holes do indeed penetrate through the film. Moreover, as a result of the very thin metal film the system according to the invention is highly resistant against mechanical stresses.

In another embodiment the thickness of the electrical insulation in the channel region amounts to several to several hundred nanometers. The thickness of the insulation layer at the upper and lower surfaces of the metal film amounts to several micrometers. The insulation layer may be applied by known processes of thin-film technology.

The material of the source and for the drain regions is Au or Ag or Cu or Ni or Al. The source and drain region may be structured as dots.

The system in accordance with the invention also includes a memory arrangement in which a plurality of vertical nano-transistors of the characteristics described in claim 1 are arranged adjacent each other on the metal film.

The method in accordance with the invention for fabricating vertical nano-transistors in accordance with claim 1 includes at least the following method steps: Forming holes in a thin metal film constituting the gate region of the transistor for providing the channel region, applying insulation material to the walls of the holes, applying insulation material on the upper and lower surface of the metal film, inserting semi-conductor material into the insulated holes for forming the semi-conductor channel region, applying contacts for forming the source and drain regions.

Embodiments of the method in accordance with the invention provide

for the formation of the holes in the metal foil by focused ion beams or by laser beams.

The insulation material is applied by thin-film technology or by vacuum filtration of a polymeric solution onto the wall of the holes and onto the upper and lower surface of the metal film.

In other embodiments of the invention the semi-conductor material which may be CuSCN or TiO_2 or PbS or ZnO or another compound semi-conductor is introduced into the holes of the metal foil by electro-chemical bath precipitation or chemical deposition or by the ILGAR process.

The fabrication method of the vertical nano-transistor arrangement in accordance with the invention is simple and adapts to the known thin-film technologies. As a result of the arrangement in accordance with the invention the fabrication method is no longer limited to predetermined temperatures.

The invention will be explained in greater detail with reference to a drawing.

The drawing depicts the fabrication steps of vertical nano-transistors in accordance with the invention which are embedded in a metal film.

Initially holes 4 of a diameter of 200 nm are formed in an Al or Cu film of 30 µm thickness by laser irradiation. Thereafter, an insulation layer 2 of organic material, e.g. Al_2O_3, ZnS, SiO_2 or inorganic material e.g. polystyrene by vacuum filtration of a polymer solution, is applied to the wall of the holes 4. The thickness of this layer 2 is 50 nm. Thereafter, an insulation layer 2 of a thickness of several micrometers is also applied to the upper and lower surface of the metal film 1 by known thin-film technologies. Following this, the insulated holes 4 in the metal film 1 are filled with CuSCN. This concludes the formation of a semi-conductor channel region 3 of a diameter of 100 nm.

As a final step, metallic contacts are applied as drain D and source S contacts.